A Two-Phase Zero-Inductor Voltage Converter for Datacenter and Server Applications

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***Abstract*—Sever power supplies and board level voltage regulators are currently the bottleneck limiting efficiency of overall server power architecture efficiency. In order to address this Google has proposed and implemented a 48 volt server architecture that brings a higher voltage level throughout the server rack to reduce distribution losses, and conversion losses upstream of the server power supply. However this change places additional burden on the board-level regulators that must now regulate from 48 volts down to below 1 volt for some components. The most common approach is a two stage approach called the "Intermediate Bus Architecture". A novel topology for an Intermediate Bus Architecture was proposed at APEC 2018. This topology featured extremely high efficiency, very simple control and low component count. However two other critical metrics for a bus converter are scability and power density. The work proposed in this paper demonstrates that the Zero-Inductor Voltage (ZIV) Converter can be easily scaled to multiple phases, and shows a very high density design while maintaining efficiency above other cutting edge solutions. The two-phase prototype achieves up to 800W/in^3 power density, 99.2% peak efficiency, and 97.9% full load efficiency for 840W output while maintaining good current sharing across all load conditions. The two-phase prototype requires no additional control, and is highly scalable to different power levels through paralleling.**

Keywords—DC-DC Converter, Datacenter, Intermediate Bus

I. Introduction

Spurred by explosive growth in the demand for computing resources, datacenters and servers have evolved rapidly in terms of distribution architecture to improve overall efficiency.

However, despite these improvements in distribution, the majority of the loss within datacenters still occurs at the server power supplies and board-level voltage regulators. In an attempt to improve this Google has proposed and implemented a 48 volt server architecture [3] that significantly reduces the distribution losses within the server rack, as well as improving the upstream conversion losses in the server PSU [4]. However, this new 48 volt supply presents a challenge when stepping down to the very low voltages required by modern processors. The most common approach is to utilize a two-stage conversion approach, such as the Intermediate Bus Architecture, where a bus converter steps the 48 volts down to a lower bus voltage which can then be more easily converted down by the point of load converter [5] [6]. The work outlined in this paper is an extension and improvement of the ZIV converter topology presented at APEC 2018 [7]. Scalability is a critical concern with the intermediate bus architecture; a single bus converter can feed several loads at varying power levels. The objective of this paper is to demonstrate that the ZIV converter is highly suitable for paralleling applications, as multiple phases are able to achieve significant performance improvements over single-phase converters due to interleaving, without requiring any additional complex control, and additionally to demonstrate the power density that can be achieved by the ZIV converter which was not covered in [7].

Table 1 Efficiency Breakdown of Server Power Supplies [1][2]

UPS	PDU	Rack-Level Converter	**Server PSU**	**VR Stage**	Overall
Traditional AC					
89.2	93.2	N/A	**75.5**	**81.6**	51.6
High-Efficiency AC					
97.1	94.0	N/A	**88.0**	**87.7**	69.9
Rack-Level 48VDC					
97.1	93.8	92.38	**91.5**	**87.7**	67.4
Facility-Level 400VDC					
95.3	96.8	N/A	**89.1**	**87.7**	72.7

II. Topology Overview

A. Operating Principles

The two-phase ZIV converter structure is in Figure 3, along with the PWM gate timing diagrams in Figure 4. The operation of the circuit is equivalent to two single-phase ZIV converters, shown in Figures 1 and 2, operating 180 degrees out of phase. This operation allows for interleaving to be achieved on the input capacitor, which sees significant RMS current during single-phase operation. As shown in [7] the input capacitor will see RMS current equal to $\sqrt{3}/4\ I_{out}$. For two-phase operation the input capacitor sees only $1/4\ I_{out}$ RMS, reducing the input capacitor loss by a factor of 3. In four-phase operation the input capacitor could be eliminated entirely. This allows for both increased efficiency, and increased density as the input capacitor is one of the physically largest components on the board, due to its high voltage stress. Current sharing is often a concern in multi-phase converters, however, the two-phase ZIV converter is connected only at the input, and output. Therefore is can

achieve very good droop current sharing with a symmetrical design, as verified by the experimental results.

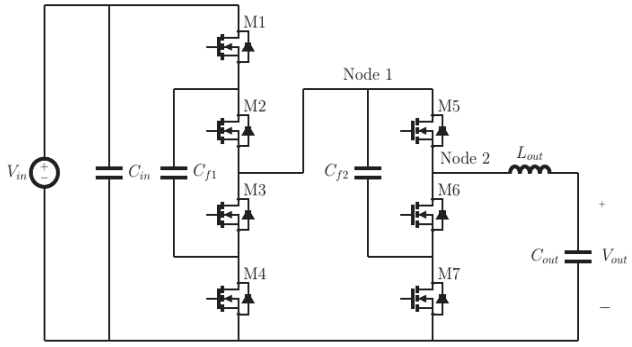

Fig. 1. Single-Phase ZIV Converter

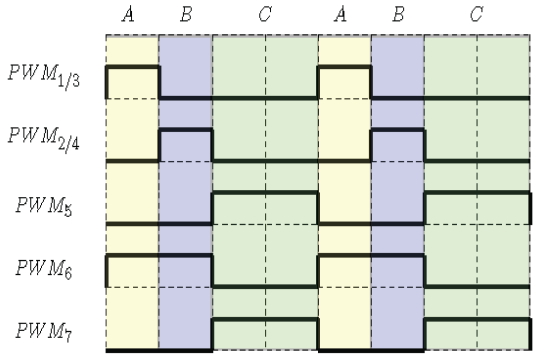

Fig. 2. Single-Phase ZIV Converter Gate Drive Diagram

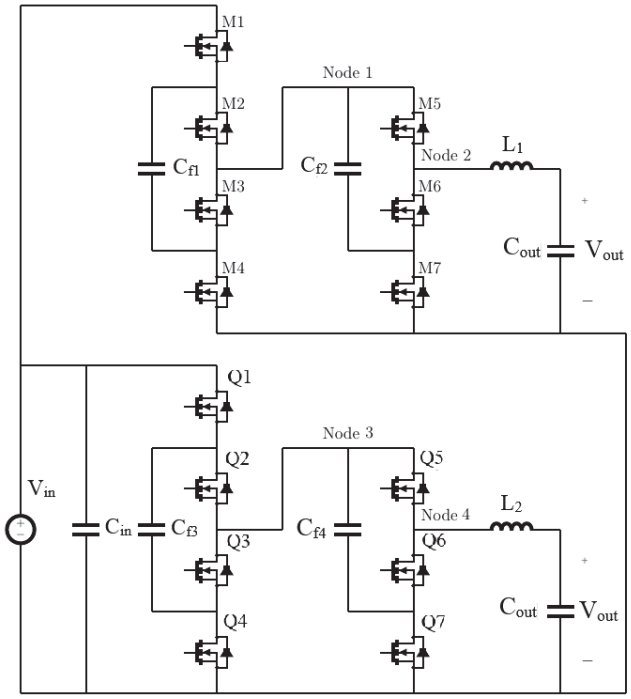

Fig. 3. Two-Phase ZIV Converter

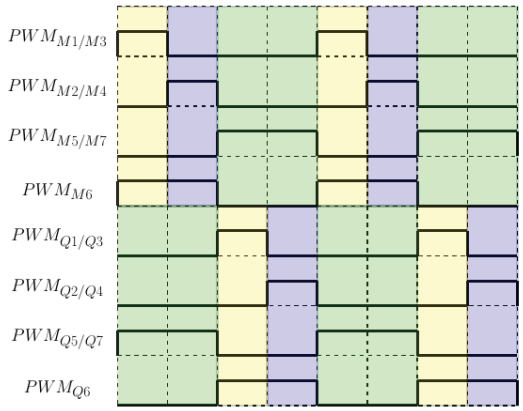

Fig. 4. Two-Phase ZIV Converter Gate Drive Diagram

B. *Input Capacitor Reduction*

As mentioned in the previous section two-phase operation significantly reduces the input capacitor RMS current compared with a single-phase ZIV converter. In the single-phase ZIV converter the input capacitor RMS is given by:

$$I_{RMS(C_{in})} = \sqrt{\left(\frac{3}{4}I_{out}\sqrt{0.25}\right)^2 + \left(\frac{1}{4}I_{out}\sqrt{0.75}\right)^2} = \frac{\sqrt{3}}{4}I_{out} \qquad (1)$$

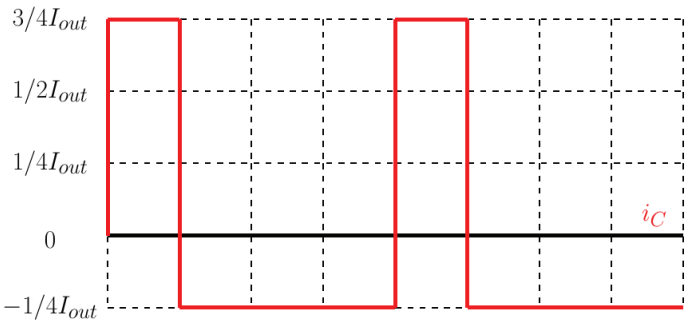

Fig. 5. Single-Phase ZIV Converter Input Capacitor Current

As shown in Figure 5 the input capacitor must discharge at 3/4 I_{out} while M1 is on, and for the remaining 75% duty cycle the capacitor charges at 1/4 I_{out}. For the two phase topology, with a 180 degree phase shift between the two phases, the input capacitor current waveform becomes the waveform shown in Figure 6. The input capacitor now effectively sees a 50% duty cycle, and charges and discharges at 1/4 of the output current, reducing the input capacitor losses by a factor of 3:

$$I_{RMS(C_{in})} = \frac{1}{4}I_{out} \qquad (2)$$

It should also be noted that in a 4-phase ZIV converter the input capacitor could be almost entirely eliminated.

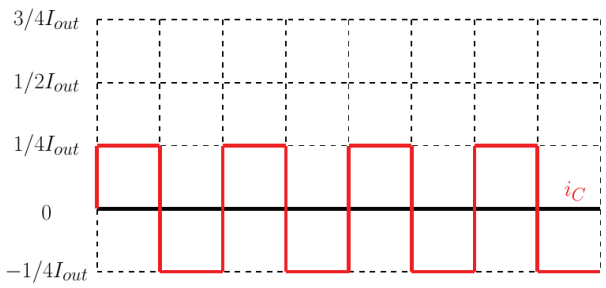

Fig. 6. Two-Phase ZIV Converter Input Capacitor Current

C. Capacitor Balancing and Start-Up

Active capacitor balancing is not required for the proposed topology. This can be demonstrated by examining the circuit in Figure 7.

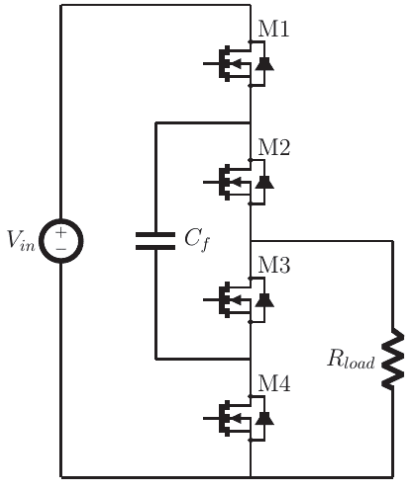

Fig. 7. Switched Capacitor "Building Block"

This circuit represents one of the four switch "building-blocks" that make up the ZIV converter. Note that for the output stages in the proposed topology, the top MOSFET (M1 in Figure 7) can be removed as it is not necessary to block the voltage at Node 1 or Node 3 from being pulled down thereby improving performance and reducing the component count. Neglecting capacitor ripple, the voltage for the capacitor can be found as follows. Let D be the duty cycle for the pair of switches M1 and M3, and let 1-D be the duty cycle for the pair of switches M2 and M4.

$$I_1 = \frac{V_{in} - V_{cap}}{R} \tag{3}$$

$$I_2 = \frac{-V_{cap}}{R} \tag{4}$$

Then by noting that for steady state the average current through the capacitor for one switching cycle must be zero:

$$I_{avg} = I_1(D) + I_2(1-D) = 0 \tag{5}$$

$$D(V_{in} - V_{cap}) = (1-D)(V_{cap}) \tag{6}$$

$$V_{cap} = DV_{in} \tag{7}$$

This demonstrates that the capacitor voltage is a function of the duty cycle, and the input voltage. Therefore there is no need for active balancing as small variations or mismatches in duty cycle will not adversely impact the circuit performance and have very little impact on the capacitor voltage.

This result is also verified in the experimental results section under Section IV-B. It should be noted that without a pre-charge circuit the MOSFETs may see voltage as high as the input voltage during startup. This is undesirable, as one of the advantages of the ZIV topology is the ability to use lower voltage rated MOSFETs to achieve higher performance. Therefore, a soft-start circuit such as in [8] is recommended unless the circuit can be started at a reduced input voltage.

III. Simulation Results

A. Key Operating Waveforms

In order to demonstrate the operation of the proposed topology simulation waveforms are presented. The simulation parameters are shown in Table 2.

Table 2 Simulation Parameters

Simulation Parameters	
Switching Frequency	60kHz
Input Voltage	48V
Load Current	30A
Deadtime	100nsec
Inductor Value	200nH
Capacitor Value	100uF

Figure 8 shows the input voltage, Node 1 voltage, and output voltage for the circuit. This demonstrates the 4:1 step-down achieved by the topology. Note that Node 1 is pulled down to the output voltage during operating state C due to the reduction to 3 switches in the output stage.

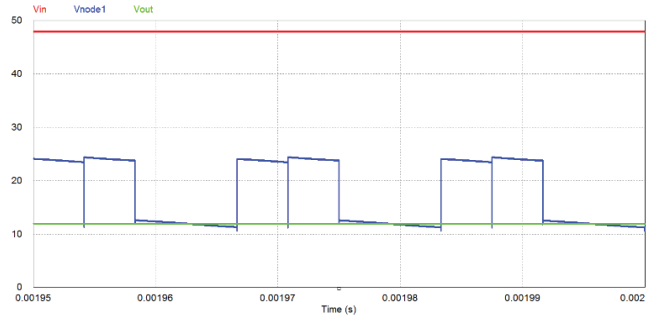

Fig. 8. Input Voltage, Output Voltage and Node 1 Voltage Waveforms

Figure 9 shows the capacitor voltage waveforms for C_{f1} to C_{f4}. This shows the two phases operating 180 degrees out of phase, as well as the reduction is MOSFET voltage stress enabled by the capacitors.

Figure 10 shows the output voltage of each phase, overlaid with the Node 2 voltage, and the Node 3 voltage in a separate plot below. This Figure demonstrates the key advantage of the

topology, namely the "zero-inductor voltage" operation is maintained in this 2-phase topology. The negative pulses on the output voltage before filtering are due to the dead-time included in the simulation, and otherwise the voltage across the inductor is only capacitor ripple. Note that the magnitude of the negative pulse during the deadtime will change depending on the switching transition, as during some transitions only one MOSFET diode will reverse conduct, and during some two MOSFET diodes will reverse conduct.

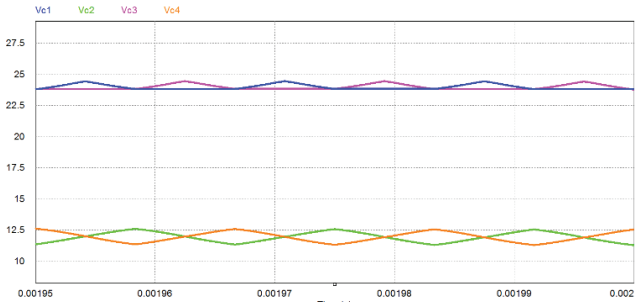

Fig. 9. Flying Capacitor Voltage Waveforms

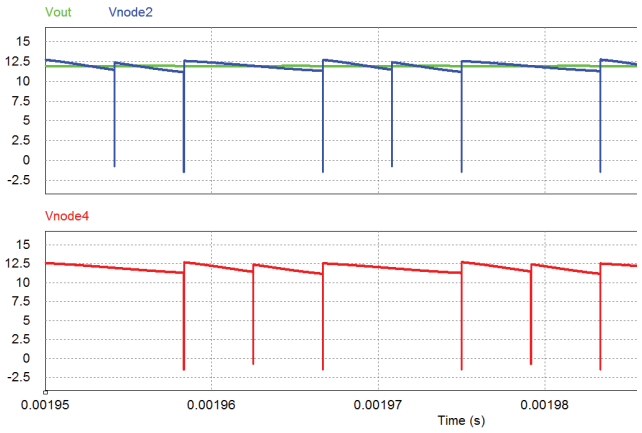

Fig. 10. Output Voltage, Node 3 and Node 4 Voltage Waveforms

The inductor current waveforms are shown in Figure 11. This shows that each phase carries one-half of the total load current. It is noted that the inductor current ripple is small despite using a 200nH inductor with only 60kHz switching frequency.

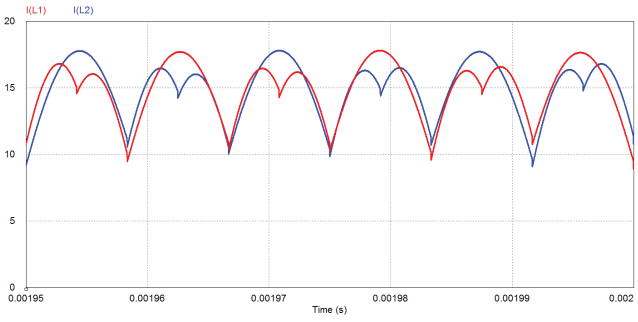

Fig. 11. Inductor Current Waveforms

B. *Capacitor Balancing*

The capacitor waveforms during start-up with no soft-start are shown in Figure 12. This simulation verifies that, without any pre-charging, the capacitors settle at their expected steady-state values with no active balancing or control required.

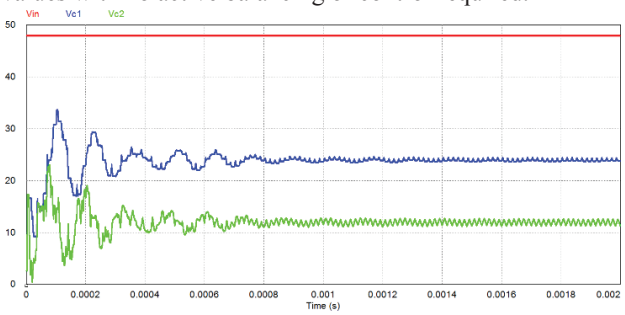

Fig. 12. Capacitor Voltage Start-Up Waveforms, No Soft-Start

IV. Experimental Results

A. *Component Selection and Loss-Breakdown*

The sources of loss in the converter must be understood in order to select the correct components. Based on the zero-inductor voltage operation of the topology the inductor value can be very small as the voltage across the inductor is only the capacitor ripple voltage. This means that the inductor loss is also hugely reduced; as shown in [7]. The inductor loss is primarily only the conduction losses related to the DCR.

The capacitors must be selected such that the voltage ripple of the capacitor does not result in any of the MOSFETs seeing a voltage that exceeds the maximum rating of the device. As the capacitor ripple is proportional to the load current, this calculation should be done utilizing the maximum load current, I_{max}. If $V_{DS}(max)$ is the maximum rating for the MOSFET, V_{cap} is the nominal voltage of the capacitor (either $1/2V_{in}$ for C_{f1} and C_{f3} or $1/4V_{in}$ for C_{f2} and C_{f4}) and t_c is the charging time of the capacitor (equal to one quarter of the switching period for C_{f1} and C_{f3} and one half of the switching period for C_{f2} and C_{f4}) then the minimum capacitor value for an n-phase ZIV converter is given by:

$$C > \frac{\frac{1}{n} I_{max} t_c}{V_{DS(max)} - V_{cap}} \tag{8}$$

Note that this is the minimum capacitor value required to avoid damaging the MOSFETs. In the practical design of a ZIV converter the capacitor ESR is a significant source of loss, and therefore, in order to optimize the efficiency of the converter, it is desirable to use several capacitors in parallel to reduce the ESR. Ceramic capacitors are desirable due to their high capacitance, small size, and low ESR. However, ceramic capacitors have a large de-rating when holding a large DC voltage (this de-rating may be up to 80% depending on the voltage rating and the size of capacitor) as well as a high tolerance (up to 20%). Therefore, in the practical case, the capacitor banks should be designed to be larger to minimize the ESR as well as provide an immunity to the non-ideality of ceramic capacitors. The design does not rely on any sensitive resonant switching operation, therefore there is a high level of

immunity to variation and non-idealities in components. An increase in capacitor voltage ripple, or inductor current ripple, would not significantly impact the operation of the converter unless the maximum ratings of the components are exceeded.

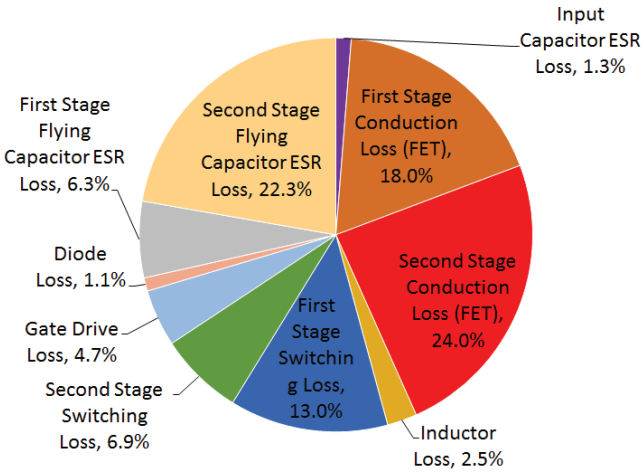

Fig. 13. Loss Breakdown for 45A Output Current

The loss breakdown for the topology, based on the components selected in Table 3, for a full-load current of 45A, is presented in Figure 13. It should be noted that the dominant source of loss in the topology, making up 74% of the total loss, is the conduction loss. The frequency related losses, such as the switching losses, gate drive losses, diode loss, are all very small because the switching frequency utilized is only 60kHz. The reduced voltage stress on the MOSFET also significantly improves the performance of the semiconductor devices. This reduction in frequency related losses is very significant as it allows the converter to achieve high performance without relying on a sensitive resonant design. Additionally, the inductor losses are minimized, comprising of almost entirely the DCR loss. As a very small inductor value is used the DCR for the inductor can also be low, much less than 1 milliohm (0.3mohm in the experimental prototype).

Over the past years the performance of semiconductor devices has rapidly improved, whereas magnetics have not seen the same level of improvement. It is therefore advantageous to eliminate the magnetics related losses, from both an efficiency and power density point of view, even at the price of using a higher number of semiconductor devices. This design philosophy has led to a large resurgence in research into switched capacitor converter-based designs in order to minimize the reliance on magnetics [9]-[14].

B. Normal Operation

A photo of the experimental prototype is shown in Figure 14. Each phase occupies an area of 1.3”x0.9” with an overall height of 0.45”. Both phases are designed symmetrically, and are “mirrors” of each other. The components selected are outlined in Table 3.

To verify the operation of the proposed topology the following waveforms are presented from the circuit operating at 30A load condition. Figure 15 shows the input voltage, Node 1 voltage, and output voltage for the converter. Figure 16 shows the Node 2 voltage demonstrating that the proposed topology maintains the “zero inductor voltage” operation, with the inductor seeing only the capacitor ripple voltage.

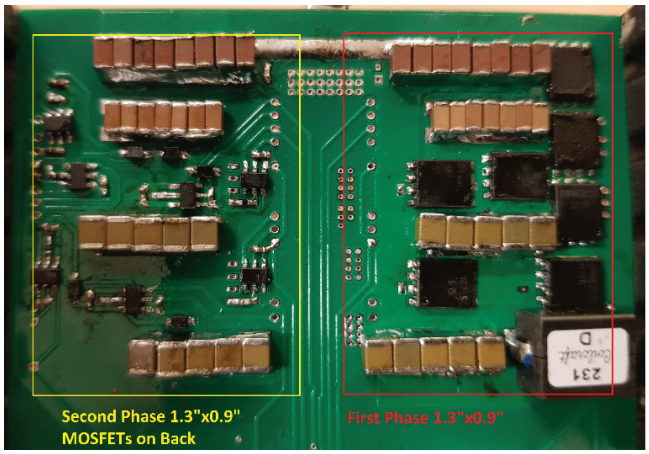

Fig. 14. Two-Phase ZIV Converter Prototype, Note that both phases are “mirrors” of each other

Table 3 Prototype Components

Circuit Prototype Parameters	
C_{in}	16x4.7uF 100V X7S 1210
C_{f1}	14x10uF 50V JB 1206
C_{f2},C_{f3}	10x47uF 25V X5R 1210
C_{out}	10x47uF 25V X5R 1210
L1, L2	230nH SLR1075-231KE
M1-M4, Q1-Q4	30V BSC011N03LSI
M5-M7, Q5-Q7	25V BSC009NE2LS5I
Switching Frequency	60kHz

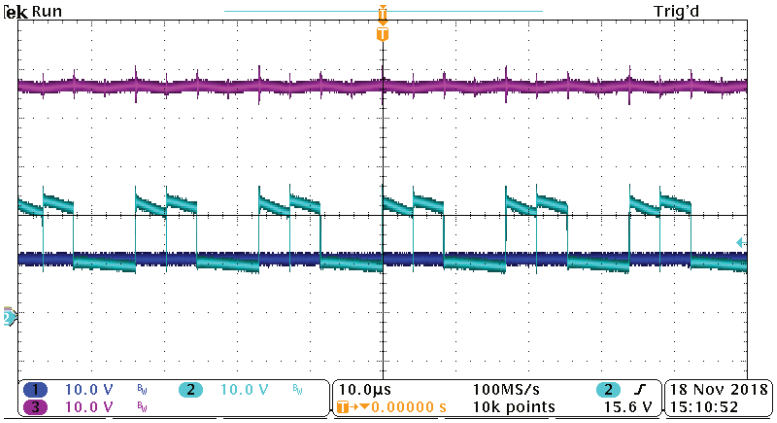

Fig. 15. Input Voltage, Node 1 Voltage, Output Voltage, 30A Load

C. Current Sharing

Figure 17 shows the AC ripple voltages for C_{f1} and C_{f2}, the flying capacitors of the first phase. Figure 18 shows the AC ripple voltages for C_{f3} and C_{f4}, the flying capacitors of the second phase. These ripple voltages are proportional to the capacitance value, and also to the current carried by each phase. The two ripple voltages presented in 17 and 18 show similar values, however some variation is expected due to the tolerance of the capacitors. Therefore, in order to verify that the current is shared evenly a thermal image of the prototype was taken.

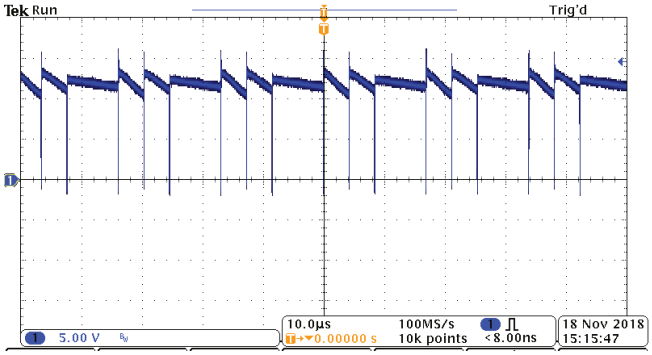

Fig. 16. Node 2 Voltage, 30A Load

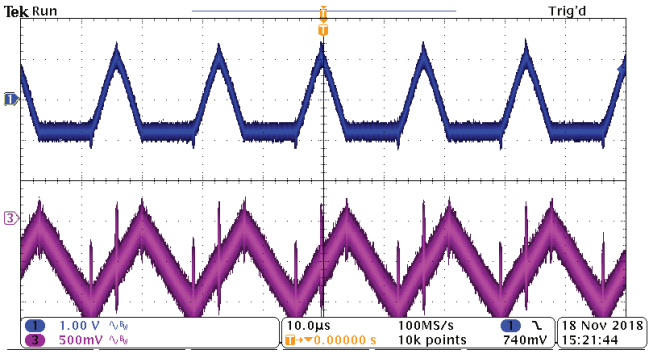

Fig. 17. C_{f1} and C_{f2} AC Ripple Voltage Waveforms, 30A Load

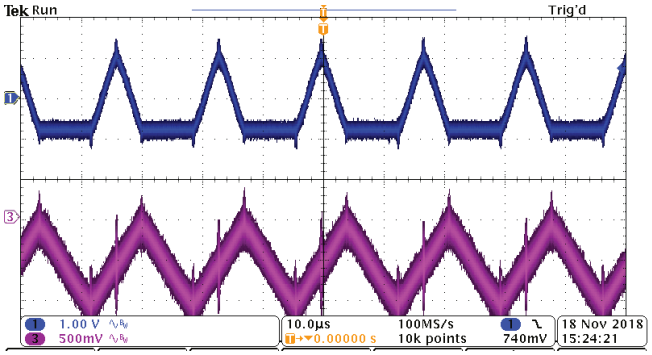

Fig. 18. C_{f3} and C_{f4} AC Ripple Voltage Waveforms, 30A Load

Figure 19 shows the thermal image of the top side of the prototype, operating at 35A load. Figure 20 shows the thermal image of the bottom side of the prototype. For 35A load both phases show very similar thermal performance, with a difference between the top and bottom phase MOSFET temperature of less than 1 degree C.

It should be noted that this current sharing performance is achieved passively. The topology provides an unregulated output voltage; therefore as the load current increases the output voltage will decrease proportionately. This allows for steady-state current sharing to be achieved without the need for additional control; the relationship between the MOSFET on-resistance and temperature provide a feedback mechanism to ensure current sharing is achieved despite device tolerances, as demonstrated here. It should also be noted that this current sharing is decided by the resistance of the circuit. Therefore the components with larger tolerances, such as the capacitance and inductor values, do not impact the current sharing.

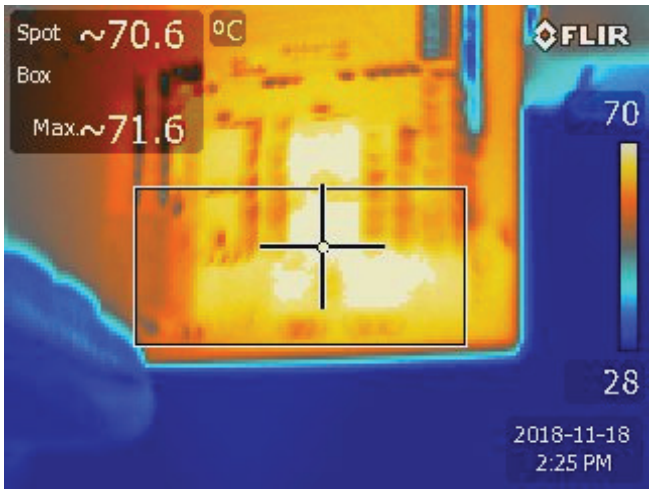

Fig. 19. Two-Phase ZIV Converter 35A Load Top Phase Thermal Image

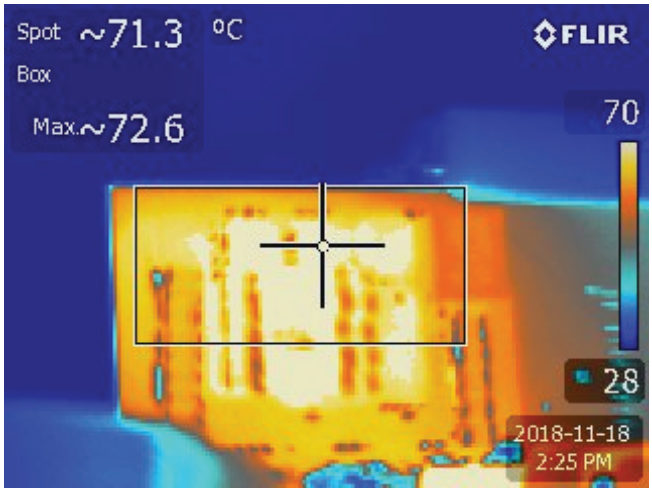

Fig. 20. Two-Phase ZIV Converter 35A Load Bottom Phase Thermal Image

D. Capacitor Balancing

A soft-start circuit is not implemented in the prototype shown in Figure 14. Therefore, the experimental procedure for starting the circuit is to slowly increase the input voltage, allowing the

capacitors to charge up to their expected value and avoiding overstressing any of the components. This start-up procedure is demonstrated in Figure 21, with the input voltage, C_{f1} and C_{f2} voltages presented. It should be noted that no active capacitor balancing or control circuitry is added to the circuit, therefore, this procedure also validates the claim that the capacitors will naturally balance near their expected value based on the duty cycle of the MOSFETs.

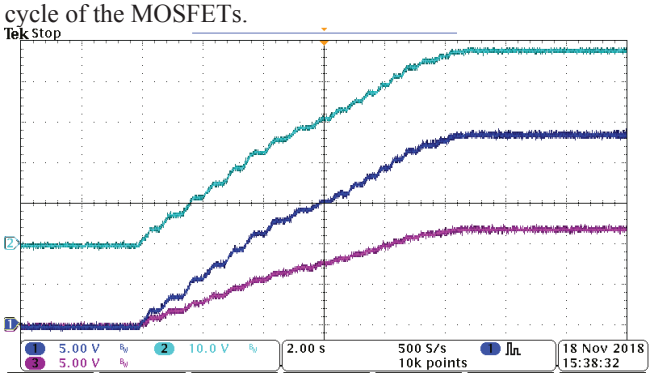

Fig. 21. Input Voltage, C_{f1} and C_{f2} Voltage Waveforms During Start-Up

E. *Efficiency Testing*

The efficiency curve for the experimental prototype is presented in Figure 22. The measurements were taken using a Keithley 2700 digital multimeter, and Reidon RSN series (0.1% error) current shunts. The prototype achieves a peak efficiency of 99.2% and a full-load, 45A or 540W, efficiency of 98.6%.

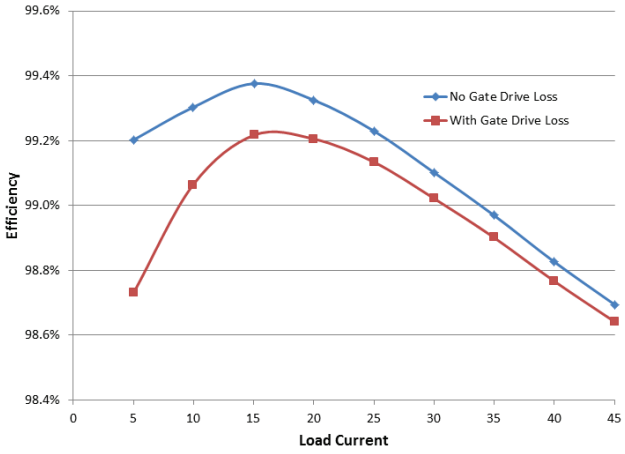

Fig. 22. Two-Phase ZIV Converter Efficiency Curve, No Cooling

A thermal image of the prototype, under 45A load current, is presented in Figure 23. From the thermal image it can be seen that the MOSFETs are the hottest components, and that both the input capacitor (left side) and inductor (top right corner) are very cool by comparison. This demonstrates the advantages of the 2-phase converter, namely that the inductor losses are significantly minimized, and also the input capacitor loss is reduced compared with a single-phase ZIV converter. This testing was conducted with no cooling or heat sink. 45A current was taken to be the maximum load current to prevent the converter temperature from exceeding 100 degrees C.

In order to achieve higher output current a second test, utilizing a small USB-powered desk fan picture in Figure 24, for cooling was conducted. The efficiency curve for the fan testing, as compared with the results using no fan, is presented in Figure 25. For both curves the gate-drive loss is included in the efficiency measurement.

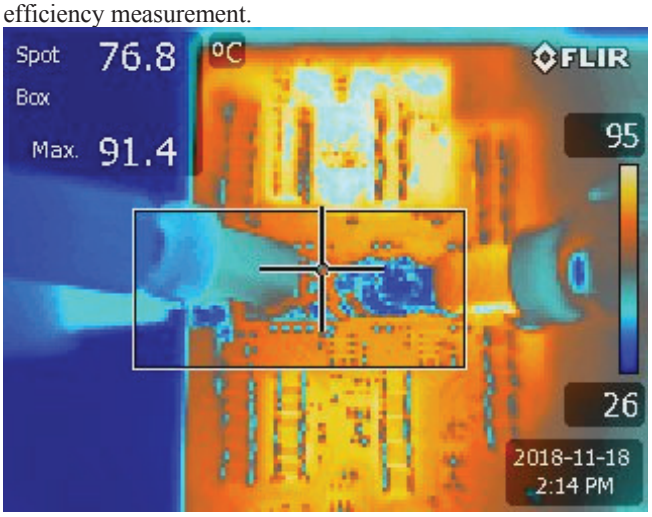

Fig. 23. Two-Phase ZIV Converter Full-Load 45A Thermal Image, No Cooling

Fig. 24. USB Desk Fan

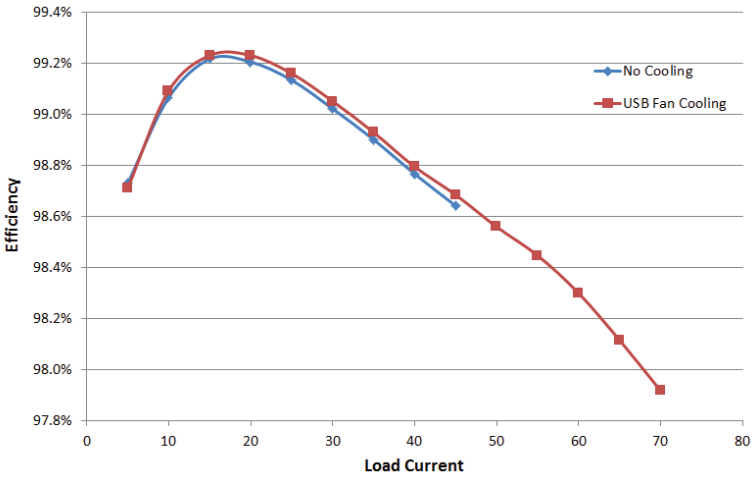

Fig. 25. Two-Phase ZIV Converter Efficiency, Gate Loss Included

The fan provides a small improvement in the performance of the circuit due to a reduction in the operating temperature of the MOSFETs. This lowers the on-resistance, reducing the conduction loss of the components. Figure 26 shows a thermal image of the converter operating at 45A with the fan cooling showing the improvement in thermal performance. Figure 27 shows the thermal image for the converter operating at the full load 70A. For the full 70A, 840W, load the converter achieves 97.9% efficiency.

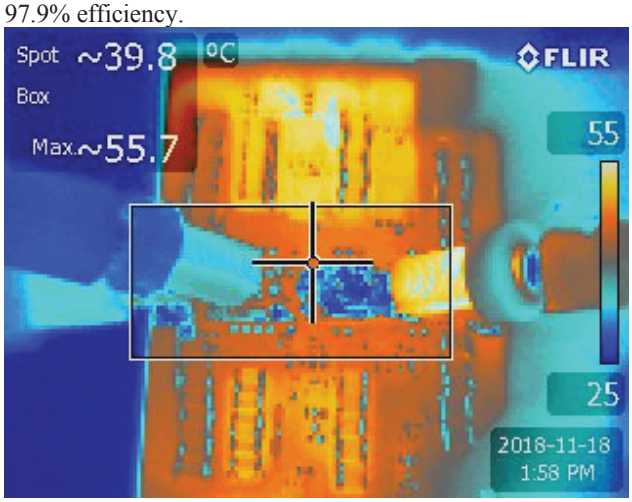

Fig. 26. Two-Phase ZIV Converter 45A Thermal Image, Fan Cooling

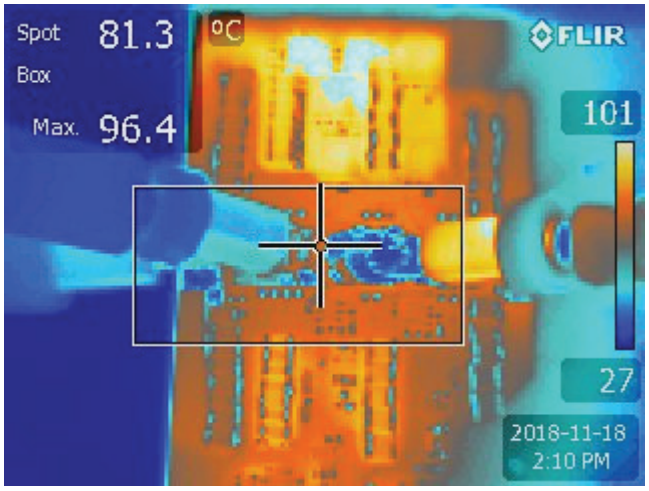

Fig. 27. Two-Phase ZIV Converter Full-Load 70A Thermal Image, Fan Cooling

V. Conclusions

The two-phase ZIV converter topology demonstrates the ability of the ZIV topology to achieve passive current sharing, enabling the topology to be scaled to varying power levels. Additionally, the interleaving of the input capacitor allows for significant reduction in the size of this bulky component as compared with a single-phase ZIV converter. The steady-state current sharing of the topology is verified by examining both capacitor ripples of the flying capacitors for each phase, as well as a thermal image of the MOSFETs. This current sharing is achieved passively. The self-balancing of the converter flying capacitors is also demonstrated in both simulation and experimental results. With no fan cooling the converter achieves a maximum of 540W output, with a full load efficiency of 98.6% and a peak efficiency of 99.2%. With the addition of USB desk fan for cooling the maximum output of the prototype was raised to 840W, with a full load efficiency of 97.9%. As each phase occupies a volume of 1.3”x0.9”x0.45” the power density of the prototype is 800W/in^3 as measured by the smallest box volume the converter could occupy. It should be noted that the off-the-shelf inductor is by far the tallest component on the board, with a height of 0.3 inches, compared with only 0.1 inches for the tallest capacitor. Therefore, by replacing this off-the-shelf inductor with a thinner magnetic component the power density of the converter could be further improved.

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